IN THE CLAIMS

Please rewrite claims 1-20, as follows:

1. (Currently amended) A semiconductor circuit designing apparatus, comprising:

a circuit design unit ~~executing~~ which executes a logical design of a semiconductor integrated circuit; and

an inspection item database section in which a circuit feature of said semiconductor integrated circuit corresponds to an inspection item of ~~a~~ an inspection to be executed before a layout design of said semiconductor integrated circuit is executed, ~~and~~

wherein said circuit design unit generates ~~a~~ target circuit feature information indicating said circuit feature of a target semiconductor integrated circuit of said semiconductor integrated circuit ~~of~~ for which said logical design should be executed, ~~and~~

wherein said circuit design unit obtains a target inspection item of said inspection item corresponding to said target circuit feature information from said inspection item database section, and

wherein said circuit design unit executes said logical design of said target semiconductor integrated circuit in reference to said target inspection item.

2. (Currently amended) ~~The semiconductor circuit designing apparatus according to Claim 1,~~ A semiconductor circuit designing apparatus, comprising:

a circuit design unit which executes a logical design of a smeiconductor integrated circuit; and

an inspection item database section in which a circuit feature of said semiconductor integrated circuit corresponds to an inspection item of an inspection to be executed before a layout design of said semiconductor integrated circuit is executed,

wherein said circuit design unit generates a target circuit feature information indicating said circuit feature of a target semiconductor integrated circuit for said semiconductor integrated circuit of which said logical design should be executed,

wherein said circuit design unit obtains a target inspection item of said inspection item corresponding to said target circuit feature information from said inspection item database section, and

wherein said circuit design unit executes said logical design of said target semiconductor integrated circuit in reference to said target inspection item, and further comprising:

a model development history database section in which ~~an~~ ID data of said circuit design unit ~~corresponds~~ is stored corresponding to a ~~the~~ number of times said circuit design unit failed said inspection of said inspection item previously, ~~and~~

wherein said target inspection item is determined such that said inspection item ~~of~~ for which said number of times is smaller than a predetermined value is withdrawn from said target inspection item.

3. (Currently amended) The semiconductor circuit designing apparatus according to Claim 1, further comprising:

a layout design unit executing said layout design, ~~and~~

wherein said circuit design unit executes said inspection of said target semiconductor integrated circuit ~~of~~ for which said layout design is executed, with regard to said target inspection item, and

wherein said circuit design unit provides a result of said inspection ~~with~~ of said target semiconductor integrated circuit to said layout design unit.

4. (Currently amended) The semiconductor circuit designing apparatus according to Claim 2, further comprising:

a layout design unit executing said layout design, ~~and~~

wherein said circuit design unit executes said inspection of said target semiconductor integrated circuit ~~of~~ for which said layout design is executed, with regard to said target inspection item, and

wherein said circuit design unit provides a result of said inspection ~~with~~ of said target semiconductor integrated circuit to said layout design unit.

5. (Currently amended) The semiconductor circuit designing apparatus according to Claim 4, wherein when said provided result of said inspection ~~has no problem,~~ does not indicate a defect, said layout design unit stores said ID data of said circuit design unit and said number of times said circuit design unit failed said inspection of said target inspection item in said model development history database section.

6. Currently amended) The semiconductor circuit designing apparatus according to Claim 1, wherein said inspection item database section ~~belongs~~ is connected to said circuit design unit.

7. (Currently amended) The semiconductor circuit designing apparatus according to Claim 2, wherein said inspection item database section ~~belongs~~ is connected to said circuit design unit.

8. (Currently amended) The semiconductor circuit designing apparatus according to Claim 3, wherein said inspection item database section ~~belongs~~ is connected to said layout design unit.

9. (Currently amended) The semiconductor circuit designing apparatus according to Claim 4, wherein said inspection item database section ~~belongs~~ is connected to said layout design unit.

10. (Currently amended) The semiconductor circuit designing apparatus according to Claim 5, wherein said inspection item database section ~~belongs~~ is connected to said layout design unit.

11. (Currently amended) The semiconductor circuit designing apparatus according to Claim 3, wherein said layout design unit includes a plurality of layout design sections, and

wherein said inspection item database section ~~belongs~~ is connected to at least one of said plurality of layout design sections.

12. (Currently amended) The semiconductor circuit designing apparatus according to Claim 3, further comprising:

a data center ~~provided to be different~~ distinct from said circuit design unit and said layout design unit,

wherein said inspection item database section ~~belongs~~ is connected to said data center.

13. (Currently amended) A semiconductor circuit designing method, comprising:

(a) providing ~~a~~ an inspection item database section in which a circuit feature of a semiconductor integrated circuit ~~in~~ for which a logical design should be executed corresponds to an inspection item of ~~a~~ an inspection to be executed before a layout design of said semiconductor integrated circuit is executed;

(b) notifying a circuit designer executing said logical design of said semiconductor integrated circuit of said inspection item corresponding to said semiconductor integrated circuit retrieved from said inspection item database section; and

(c) executing said logical design of said semiconductor integrated circuit by said circuit designer ~~in~~ with reference to said notified inspection item.

14. (Currently amended) The semiconductor circuit designing method according to Claim 13, further comprising:

(d) providing said semiconductor integrated circuit ~~in~~ for which said notified inspection item is ~~passed~~ satisfactory ~~to~~ with a layout designer executing said layout design.

15. (Currently amended) ~~The~~ A semiconductor circuit designing method, comprising:

~~(e)~~ (a) providing a circuit design unit executing a logical design of a semiconductor integrated circuit; and

~~(f)~~ (b) providing an inspection item database section in which a circuit feature of said semiconductor integrated circuit corresponds to an inspection item of ~~a~~ an inspection to be executed before a layout design of said semiconductor integrated circuit is executed, ~~and~~

wherein said circuit design unit generates a target circuit feature information indicating said circuit feature of a target semiconductor integrated circuit of said semiconductor integrated circuit ~~of~~ for which said logical design should be executed, ~~and~~

wherein said circuit design unit obtains a target inspection item of said inspection ~~item~~ item, said target inspection item corresponding to said target circuit feature information from said inspection item database section, and

wherein said circuit design unit executes said logical design of said target semiconductor integrated circuit ~~in~~ with reference to said target inspection item.

16. (Currently amended) ~~The semiconductor circuit designing method according to Claim 15,~~ A semiconductor circuit designing method, comprising:

(a) providing a circuit design unit executing a logical design of a smeiconductor integrated circuit; and

(b) providing an inspection item database section in which a circuit feature of said semiconductor integrated circuit corresponds to an inspection item of an inspection to be executed before a layout design of said semiconductor integrated circuit is executed,

wherein said circuit design unit generates target circuit feature information indicating said circuit feature of a target semiconductor integrated circuit of said semiconductor integrated circuit for which said logical design should be executed,

wherein said circuit design unit obtains a target inspection item of said inspection item, said target inspection item corresponding to said target circuit feature information from said inspection item database section, and

wherein said circuit design unit executes said logical design of said target semiconductor integrated circuit with reference to said target inspection item, and further comprising:

~~(g)~~ (c) providing a model development history database section in which ~~an~~ ID data of said circuit design unit corresponds to ~~the~~ a number of times said circuit design unit failed said inspection of said inspection item previously,

wherein said target inspection item is determined such that inspection item for which said number of times is smaller than a predetermined value is withdrawn from said target inspection item.

17. (Currently amended) The semiconductor circuit designing method according to Claim 15, further comprising:

~~(h)~~ (d) providing a layout design unit executing said layout design, ~~and~~

wherein said circuit design unit executes said inspection of said target semiconductor integrated circuit ~~of~~ for which said layout design is executed, with regard to said target inspection item, and

wherein said circuit design unit provides a result of said inspection ~~with~~ of said target semiconductor integrated circuit to said layout design unit.

18. (Currently amended) The semiconductor circuit designing method according to Claim 16, further comprising:

~~(i)~~ (e) providing a layout design unit executing said layout design, ~~and~~

wherein said circuit design unit executes said inspection of said target semiconductor integrated circuit ~~of~~ for which said layout design is executed, with regard to said target inspection item, and

wherein said circuit design unit provides a result of said inspection ~~with~~ of said target semiconductor integrated circuit to said layout design unit.

19. (Currently amended) The semiconductor circuit designing method according to Claim 18, wherein when said provided result of said inspection ~~has no problem,~~ does not indicate a defect, said layout design unit stores said ID data of said circuit design unit and said number of times said circuit design unit failed said inspection of said target inspection item in said model development history database section.

20. (Currently amended) The semiconductor circuit designing method according to Claim 15, wherein said inspection item database section ~~belongs~~ is connected to said circuit design unit.